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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,086	11/26/2003	Hirofumi Shibuya	XA-9985	7814

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,086	SHIBUYA ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 8-10 disclose "substitutes the area during an idle state causing no operations in the storage device when the area is assumed to be a critical state".

This language does not allow one of ordinary skill in the art to determine the scope of the claimed invention. For purposes of this action, the "during an idle state causing no operations in the storage device" part of this limitation will be ignored.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosono et al (US PGPub No. 2003/0169630) and Harari et al (US Patent No. 5,991,517).

For claim 1, Hosono discloses a storage device comprising one or more semiconductor memories (a nonvolatile semiconductor memory device, par. 0012) and an information processing section which reads data stored in the one or more semiconductor memories based on an operating program and instructions.a predetermined process and an operation to write data (a data read/write circuit arranged to perform data read of the memory cell array and data write to the memory cell array, par. 0015),

wherein the information processing section detects a state of an area in the semiconductor memory (the control circuit performs control of status registers, par. 0048).

Hosono does not, however, expressly disclose substituting the area when the area is assumed to be a critical state, or substituting the area immediately when the area is assumed to be a limit state.

Harari, however, discloses error correction code (ECC) is employed at all times to correct for soft errors as well as any hard errors that may arise. As soon as a hard error is detected, defect mapping is used to replace the defective cell with a spare cell in the same sector block. Only when the number of defective cells in a sector exceeds the defect mapping's capacity for that specific sector will the whole sector be replaced as in a conventional disk system (col. 10, lines 43-50).

Harari and Hosono are analogous art in that they are of the same field of endeavor, that is, a system and method for semiconductor memory management, especially for the handling of data reading and writing. It would have been obvious to a

person of ordinary skill in the art at the time of the invention to implement a distinction between limit and critical states and substitute the applicable areas in the appropriate manner because this scheme minimizes wastage without compromising reliability (col. 10, lines 50-52), as taught by Harari.

For claim 2, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses a factor for the information processing section to determine a critical state comprises one or more of an insufficiency of a substitute free area, a successive retry error, a time over of an erasure time or a program time, an erasure count, an over current of performing a read operation or a write operation, and a less current value of externally supplied power and wherein a factor for the information processing section to determine a limit state comprises one or more of an insufficiency of a substitute free area, a successive retry error, an ECC uncorrectable error at retention failure, a device code unreadable error, a time over of an erasure time or a program time, an erasure count, an over current of performing a read operation or a write operation, and a less current value of externally supplied power (defective cells are detected by their failure to program or erase correctly. Also during read operation, defective cells are detected and located by the ECC, col. 10, lines 33-36; as soon as an error is detected, defect mapping is used to replace the defective cell with a spare cell in the same sector block. Only when the number of defective cells in a sector exceeds the defect mapping's capacity for that specific sector will the whole sector be replaced, col. 10, lines 45-50).

For claim 3, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses independently setting the factors for the information processing section to determine a critical state and setting the factors for the information processing section to determine a limit state (the multiple threshold breakpoint levels are provided by a set of memory cells which serves as master reference cells, which are independently and externally programmable, either by the memory manufacturer or the user, col. 3, lines 1-6).

For claim 4, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses a substitution destination area substituted by the information processing section is a free area in the semiconductor memory or semiconductor memory for substitution only (the memory architecture has a typical sector organized into a data portion and a spare or shadow portion. The data portion is memory space available to the user. The spare portion is further organized into an alternative defects data area, a defect map area, a header area and an ECC and others area, col. 10, lines 56-62 and fig. 5, items 405-413).

For claim 5, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses the substitution destination area is a free area in the semiconductor memory, the substitution destination area is a physical area controlled by an individual peripheral circuit which controls any of a plurality of sectors provided for a memory mat (a memory device which may include a plurality of memory chips is under the control of the controller,

which is itself part of a microcomputer system under the control of a microprocessor, col. 11, lines 22-25 and fig. 6, item 31).

For claim 6, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses a decode method of the device substitutes only data in a substitution origin area for data in a substitution in a substitution destination area, after substitution, allows access to the substitution destination area instead of the substituted area, and allows access to an unsubstituted area in the same manner as before the substitution (when the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to the defective sector is denied and the substitute address present in the defect map is entered, and the corresponding substitute sector is accessed instead. The sector remapping is performed by a microprocessor. The microprocessor looks at the incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitutes the alternative location as the new command, col. 14, lines 14-25).

For claim 7, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Hosono further discloses the information processing section notifies an outside (a data output operation from the data read/write circuit to outside of a chip and a data write operation from the data read/write circuit to the memory cell array are overlapped with each other, par. 0016).

Hosono does not, however, expressly disclose this notification of an outside is for an emergency condition when determining that the area is in a limit state.

Harari, however, discloses determining this limit state for an area (defect mapping is used to replace the defective cell with a spare cell in the same sector block. Only when the number of defective cells in a sector exceeds the defect mapping's capacity for that specific sector will the whole sector be replaced as in a conventional disk system, col. 10, lines 43-50).

Harari and Hosono are analogous art in that they are of the same field of endeavor, that is, a system and method for semiconductor memory management, especially for the handling of data reading and writing. It would have been obvious to a person of ordinary skill in the art at the time of the invention to notify an outside when a limit state is determined for an area because this would allow for greater system awareness, and would enable different correctional options to adequately rectify the few errors that may crop up in the system (col. 2, lines 41-43), as taught by Harari.

5. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosono et al (US PGPub No. 2003/0169630), Harari et al (US Patent No. 5,991,517) and Schwarz (US Patent No. 6,496,947).

For claim 8, the combined teachings of Hosono and Harari disclose the invention as per the rejection of claim 1 above. Harari further discloses determining a limit state for an area as per the rejection of claim 7 above.

Harari does not, however, disclose restricting operations such as inhibiting a write operation are performed when a limit state is determined.

Schwarz, however, discloses a built-in test circuit coupled to the memory array for executing a sequence of write and read operations on the memory array, and a pause circuit coupled to and activated by the built-in self test means for pausing the sequence of read and write operations (col. 2, lines 30-34).

Schwarz, Hosono and Harari are analogous art in that they are of the same field of endeavor, that is, a system and method for semiconductor memory management, especially for the testing and reading/writing operations for such. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include inhibiting a write operation when a limit state is determined because this pause ensures that there is at least a predetermined delay between accesses in subsequent runs through a memory array, and allow for sufficient length of time to pass between subsequent memory accesses such that a testing circuit may detect and repair data retention faults from cells having relatively short leakage times (col. 4, lines 60-63), as taught by Schwarz.

For claim 9, the combined teachings of Hosono and Harari disclose the invention as per claim 1 above. Harari further discloses the information processing section copies data from a substitution origin area to a substitution destination area during the area substitution, as per rejection of claim 6 above.

The combined teachings of Hosono and Harari do not, however, expressly disclose correcting of a correctable error if it is contained in the data.

Schwarz, however, discloses a compare circuit which compares actual data read from the cell with the expected data and notifies a testing circuit of any errors, which are

either repaired through address re-mapping circuit or, if the error cannot be repaired, the testing circuit activates a fail flag (col. 6, lines 66-67 and col. 7, lines 1-5).

Schwarz, Hosono and Harari are analogous art in that they are of the same field of endeavor, that is, a system and method for semiconductor memory management, especially for the testing and reading/writing operations for such. It would have been obvious to a person of ordinary skill in the art at the time of the invention to including correcting of a correctable error after substitution because this ensures the memory should be fully functional and reliable (col. 7, lines 37-40), as taught by Schwarz.

Claim 10 is rejected using the same rationale as for the rejections of claims 1, 6, 7 and 8 above.

Contact Information

6. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions

regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

11-22-05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER